Claims:

1. A system for evaluating a semiconductor device pattern, comprising:

feature index calculating means for quantifying a property of a three-dimensional shape of each pattern to be evaluated, as feature index;

database storing means for storing a database that records therein a relationship between feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index; and

device property estimating means for estimating properties of a device circuit formed by the pattern to be evaluated, on the basis of the feature indices of the three-dimensional pattern shape, which have been quantified by said feature index calculating means, and the information recorded in the database stored in said database storing means.

2. A system for evaluating a semiconductor device pattern, comprising:

feature index calculating means including,

electron beam irradiating means for irradiating a converged electron beam onto a pattern to be evaluated, while scanning the same;

secondary electron detecting means for detecting secondary electrons produced from the pattern by the irradiation of the electron beam by said electron beam irradiating means; and

signal arithmetic processing means for dividing a signal waveform of the secondary electrons detected by said secondary electron detecting means into a plurality of regions, based on an amount of change in signal amount, and quantifying a property of a three-dimensional shape of the pattern to be evaluated, as a feature index on the basis of the size of said each divided region;

database storing means for storing a database that records therein a relationship between feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index; and

device property estimating means for estimating a property of a device circuit formed by the pattern to be evaluated, on the basis of the feature indices of the three-dimensional pattern shape quantified by said feature index calculating means, and the information recorded in the database.

3. The system according to claim 2, wherein said secondary electron detecting means detects a plurality of secondary electrons different in angle formed by the

electron beam irradiated from said electron beam irradiating means and the surface of the pattern to be evaluated.

4. The system according to claim 2, further including back scattered electron detecting means for detecting back scattered electrons produced from the pattern by the irradiation of the electron beam by said electron beam irradiating means, wherein said signal arithmetic processing means quantifies a property of the three-dimensional shape of the pattern as a feature index on the basis of a signal of the secondary electrons detected by said secondary electron detecting means, and a signal of the back scattered electrons detected by said back scattered electron detecting means.

5. The system according to claim 1, wherein said device property estimating means evaluates the degree of similarity between the feature indices of the three-dimensional shape of the pattern, which have been quantified by said a feature index calculating means, and the feature indices of each three-dimensional pattern shape, which have been recorded in the database, and estimates device properties of a circuit containing patterns each having a feature index high in the degree of similarity, as the properties of the device circuit formed by the pattern to be evaluated.

6. The system according to claim 1, wherein said device property estimating means estimates the three-dimensional pattern shape, based on the feature indices of the three-dimensional pattern shape, which have been calculated by said feature index calculating means, and estimates the properties of a device circuit formed by the pattern to be evaluated, based on feature indices of a three-dimensional shape at an arbitrary specific point, of the estimated three-dimensional pattern shape.

7. The system according to claim 1, wherein said device property estimating means represents a relationship between the feature indices of each three-dimensional pattern shape, which have been recorded in the database, and the device properties of a circuit containing patterns each having the feature index in the form of a function by a regression analysis, and estimates the properties of the device circuit formed by the pattern to be evaluated, on the basis of the function and the feature indices of the three-dimensional pattern shape, which have been quantified by said feature index calculating means.

8. The system according to claim 1, wherein said device index estimating means represents a relationship between the feature indices of each three-dimensional pattern shape, which have been recorded in the database, and the device properties of a circuit containing patterns

each having the feature index by information about the strength of a relationship of the respective device property with respective three-dimensional pattern shape feature index determined by a regression analysis, and estimates the properties of a device circuit formed by the pattern to be evaluated, on the basis of the information and the feature indices of the three-dimensional pattern shape, which have been quantified by said feature index calculating means.

9. A method for evaluating a semiconductor device pattern, comprising the following steps of:

quantifying a property of a three-dimensional shape of a pattern to be evaluated, as feature index;

recording a relationship between said quantified feature indices of three-dimensional pattern shape, and device properties of a circuit including patterns each having the feature index, and storing the result of recording as a database; and

estimating properties of a device circuit formed by the pattern to be evaluated, on the basis of said quantified feature indices of three-dimensional pattern shape and information recorded in the stored database.

10. A method for evaluating a semiconductor device pattern, comprising the following steps of:

irradiating a converged electron beam onto a pattern

to be evaluated, while scanning the same;

detecting secondary electrons produced from said pattern by the irradiation of the electron beam;

dividing a signal waveform obtained by the detection of the secondary electrons into a plurality of regions, based on an amount of change in signal amount of the signal waveform;

quantifying properties of a three-dimensional shape of the pattern to be evaluated, as a feature index on the basis of the size of said each divided region; and

estimating properties of a device circuit formed by the evaluated pattern from said quantified feature indices of pattern to be evaluated, on the basis of a relationship between pre-stored feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index.

11. The method according to claim 10, wherein in said irradiating step, the electron beam is irradiated onto the evaluated pattern from different plural directions.

12. The method according to claim 10, wherein in a step for, in said detecting step, further detecting back scattered electrons generated from the pattern to be evaluated and dividing the same into the plurality of regions, a waveform division is done based on an amount of change in signal amount of the signal waveform obtained by

detecting the secondary electrons, and an amount of change in signal amount of a signal waveform obtained by detecting the back scattered electrons, and in said quantifying step, the properties of the three-dimensional pattern shape is quantified as a feature index on the basis of a signal obtained by detecting the secondary electrons, and a signal obtained by detecting the back scattered electrons.

13. The method according to claim 10, wherein in said device-circuit property estimating step, the degree of similarity between the feature indices of the three-dimensional pattern shape, which have been quantified in said quantifying step, and the pre-stored feature indices of each three-dimensional pattern shape is evaluated to thereby estimate device properties of a circuit containing a pattern having a feature index high in the degree of similarity as the property of the device circuit formed by the pattern to be evaluated.

14. The method according to claim 10, wherein in said device-circuit property estimating step, the three-dimensional shape of the pattern to be evaluated is estimated based on the feature indices of the three-dimensional pattern shape, which have been quantified in said quantifying step, and the properties of a device circuit formed by the pattern to be evaluated is estimated based on feature indices of a three-dimensional pattern

shape at an arbitrary specific point, of the estimated three-dimensional pattern shape.

15. The method according to claim 10, wherein in said device circuit property estimating step, a relationship between the pre-stored feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index is represented in the form of a function by a regression analysis, and the property of a device circuit formed by the pattern to be evaluated is estimated on the basis of the function and the feature indices of the three-dimensional pattern shape, which have been quantified in said quantifying step.

16. The method according to claim 10, wherein in said device circuit property estimating step, a relationship between the pre-stored feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index is represented by information about the strength of a relationship of the respective device properties with respective three-dimensional pattern shape feature indices determined by a regression analysis, and the properties of a device circuit formed by the pattern to be evaluated is estimated on the basis of the information and the quantified feature indices of the three-dimensional pattern

shape.

17. A method for controlling a pattern forming process, comprising the following steps of:

recording in advance a relationship between feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index;

setting a target value and a tolerance level of a three-dimensional shape of a pattern necessary to realize a desired device property; and

controlling a pattern forming process using the difference between the target value and feature indices of a three-dimensional shape of a pattern to be evaluated, and the tolerance level.

18. A process monitoring method comprising the following steps of:

recording in advance a relationship between feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index;

setting a tolerance level of a three-dimensional shape of a pattern necessary to realize a desired device property, based on information about the recorded relationship; and

monitoring the presence or absence of an anormality

of a pattern forming process, based on the calculated tolerance level and feature indices of a three-dimensional shape of a pattern to be evaluated.